Notice of Allowability	Application No.	Applicant(s)	
	09/575,456	CULLUM ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communications filed 4 April 2005*.

2. ☒ The allowed claim(s) is/are *1,2,5,6,10-13,15,16,19,20,24-27,29,30,33,34,38-43,45-47 and 49-52*.

3. ☒ The drawings filed on *12 June 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *05022005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Notice of Appeal Filed 02/02/2005, Appeal Brief Filed 04/04/2005.

Allowable Subject Matter

2. Claims 1, 2, 5, 6, 10-13, 15, 16, 19, 20, 24-27, 29, 30, 33, 34, 38-43, 45-47 and 49-52 allowed.

3. The application having been allowed, formal drawings are required in response to this Office Action.

REASONS FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance: The applicant's proposed amendments further distinguish the claimed invention by including claim language that links the claimed the "applied clock signal" to the "first clock signal". Independent claim 41 has not been amended because it contains the distinguishing claim language.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Salvatore P. Tamburo, Reg. No. 45,153 on 28 April 2005.

6. The application has been amended as follows:

a. In the claims, please amend the claims as follows:

1. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing said [[a]] respective applied ~~delayed first~~ clock ~~signal~~ signals to [[a]] respective ~~one~~ ones of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

15. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing said [[a]] respective applied ~~delayed first~~ clock ~~signal~~ signals to [[a]] respective ~~one~~ ones of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

29. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing said [[a]] respective applied ~~delayed first~~ clock ~~signal~~ signals to [[a]] respective ~~one~~ ones of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

49. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each of said output circuits operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing said [[a]] respective applied ~~delayed first~~ clock ~~signal~~ signals to [[a]] respective ~~one~~ ones of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

50. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each of said output circuits operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing said [[a]] respective applied ~~delayed first~~ clock ~~signal~~ signals to [[a]] respective ~~one~~ ones of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

51. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal; and

a plurality of adjustable delay circuits for receiving said first clock signal, each of said adjustable delay circuits providing said [[a]] respective applied ~~delayed first~~ clock ~~signal~~ signals to [[a]] respective ~~one~~ ones of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming such that each of said respective data signals is output by said plurality of output circuits at substantially the same time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
May 2, 2005

LYNNE H. BROWNE
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